TITLE

METHOD OF FORMING A CAPACITOR DIELECTRIC STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a deep trench capacitor of a dynamic random access memory (DRAM) cell and, more particularly, to a method of forming a capacitor dielectric structure to enhance the capacitance of the deep trench capacitor.

Description of the Related Art

There is much interest in reducing the size of individual semiconductor devices in order to increase their density on an integrated circuit (IC) chip and thereby reduce size and power consumption of the chip, and allow faster operation. In order to achieve a memory cell with a minimum size, the gate length in a conventional transistor must be reduced to decrease the lateral dimension of the memory cell. However, the shorter gate length will result in higher leakage currents that cannot be tolerated, and the voltage on the bit line must therefore also be scaled down. This reduces the charges stored on a storage capacitor, and thus requires a larger capacitance to ensure that stored charges are sensed correctly. Recently, in fabricating highly-integrated memory devices, such as dynamic random access memory (DRAM), a deep trench capacitor has been developed within a silicon substrate without consuming any additional wafer area.

In order to prolong the data retention time, the capacitance of the storage capacitor must be increased by either increasing the capacitor area, decreasing the effective dielectric thickness between the capacitor plates, or increasing the dielectric constant (k) of the capacitor dielectric. However, increasing the capacitor area conflicts with the need to shrink the memory cell, and reducing the dielectric thickness is difficult because the dielectric thickness has already been reduced to a practical minimum. Therefore, improving the capacitor dielectric with a high dielectric constant is a way to provide adequate capacitance in view of shrinking cell size. In a conventional method, a multi-layered oxide/nitride/oxide structure, serving as an ONO structure, is employed as the capacitor dielectric. Because the dielectric constant of the silicon nitride (k=7.6) is 1.5~2 times larger than that of the silicon oxide (k=3.9), the nitride layer in the ONO structure can increase the capacitance of the deep trench capacitor. The oxide layer in the ONO structure is employed to repair the damaged interface. Nevertheless, the critical thickness of the ONO structure has a limitation of 5~10 nm, the dielectric constant of the ONO structure only reaches approximately 7, and problems of difficult process, low yield, high process cost, and leakage current occur.

Recently, a stacked nitride/oxide layer, serving as a NO structure, has been employed to form the capacitor dielectric. Fig. 1 is a sectional diagram showing a conventional deep trench capacitor. A DRAM cell comprises a transistor 22 and a deep trench capacitor 20 having a bottom

electrode plate 14, a capacitor dielectric layer 16 and an upper electrode plate 18. The bottom electrode plate 14 can be formed from the n^+-doped region in a silicon substrate 10 surrounding a deep trench 12 or from a doped-polysilicon layer that conformally covers the sidewall and the bottom of the deep trench 12. The capacitor dielectric layer 16, a NO structure, comprises a SiN liner deposited on the sidewall and bottom of the deep trench 12 by low pressure vapor deposition (LPCVD) and thin oxide layer grown on the SiN liner by oxidation process. The upper electrode plate 18 is formed by filling the deep trench 12 with a conductive layer.

In the NO structure, the SiN liner of 40~80Å thickness has the dielectric constant 1.5~2 times larger than the dielectric constant of the oxide layer of 3 nm thickness, thus the capacitance of the deep trench capacitor 20 is effectively increased. However, there is still a problem of leakage current caused by the SiN liner. Also, during deposition of the SiN liner, the used gases, such as SiH_4 and NH_3, cause defects of pinhole structures in the SiN liner. Although the oxide layer grown on the SiN liner can repair the defects, decrease the pinhole density and reduce leakage current to achieve a preferred distribution of breakdown voltage, the SiN liner is too thin to increase the dielectric constant of the NO structure. Thus, a method of increasing the dielectric constant of the capacitor dielectric layer 16 without exceeding the thickness limitation to solve the aforementioned problems is called for.

SUMMARY OF THE INVENTION

The present invention provides a method of forming a capacitor dielectric structure that is a NO structure with a nitride layer to increase the dielectric constant and ensure the electrical reliability of the capacitor dielectric structure.

The method of forming capacitor dielectric structure, comprises steps of providing a semiconductor substrate having at least a predetermined capacitor structure, using silicon nitride deposition to form a SiN layer on the predetermined capacitor structure, using a reoxidation process to grow an oxide layer on the SiN layer, and using a nitridation process to form a nitridation layer on the oxide layer.

Accordingly, it is a principle object of the invention to provide a method of forming a capacitor dielectric structure that may be applied to the formation of a deep trench capacitor or a stacked capacitor in DRAM.

It is another object of the invention to provide a nitridation layer on a NO structure to increase the dielectric constant of the capacitor dielectric structure.

Yet another object of the invention is to provide a nitridation layer on a NO structure to ensure the electrical property of the capacitor dielectric structure.

It is a further object of the invention to provide the capacitor dielectric structure to enhance capacitance of a deep trench capacitor.

Still another object of the invention is to provide the capacitor dielectric structure to prolong data retention time

of a deep trench capacitor

Another object of the invention is to provide the capacitor dielectric structure to improve electrical properties of a deep trench capacitor

It is an object of the invention to provide the capacitor dielectric structure to increase yield.

These and other objects of the present invention will become readily apparent upon further review of the following specification and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional diagram showing a conventional deep trench capacitor.

Figs. 2A to 2D are sectional diagrams showing the method of forming the capacitor dielectric structure according to the present invention.

Fig. 3 is a flow diagram showing the method of forming the capacitor dielectric structure according to the present invention.

Similar reference characters denote corresponding features consistently throughout the attached drawings.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method of forming a capacitor dielectric structure, which may be applied to the formation of a deep trench capacitor or a stacked capacitor in DRAM device. The capacitor dielectric structure is a NO structure with a nitride layer to increase the dielectric constant and ensure the electrical reliability of the capacitor dielectric structure.

In the preferred embodiment, the method is applied to the deep trench capacitor process as shown in Figs. 2 and 3. Figs. 2A to 2D are sectional diagrams showing the method of forming the capacitor dielectric structure according to the present invention. Fig. 3 is a flow diagram showing the method of forming the capacitor dielectric structure according to the present invention. As shown in Fig. 2A, a semiconductor substrate 30 is provided with a deep trench 32 formed depending on process designs and requirements. For example, using photolithography and etching, a plurality of deep trenches in array is formed in the p-type silicon substrate 30, thus the protruding portion of the silicon substrate 30 serves as pillar regions 34. Then, after successively depositing an ASG layer and an oxide layer on the sidewall of the deep trench 32, high-temperature annealing is used in a short term to diffuse As ions of the ASG layer into the silicon substrate 30, resulting in a n^+ diffusion region 36 in pillar region 34 surrounding the deep trench 32. The n^+ diffusion region 36 serves as a bottom electrode layer of a deep trench capacitor.

Next, at a step 100, a pre-cleaning process is used to clean the deep trench 32. Thereafter, at a step 200, silicon nitride deposition with 650~800℃ deposition temperature is used to form a SiN layer 38 on the sidewall and bottom of the deep trench 32 as shown in Fig. 2B. Then, at a step 300, a reoxidation process using any rapid heating method is employed to grow an oxide layer 40 on the SiN layer 38 as shown in Fig. 2C. Preferably, the SiN layer 38 is 2.8nm thick, and

the oxide layer 40 1.2nm thick.

Finally, at a step 400, a nitridation process with a temperature more than 700℃, a process time more than 30 minutes and gases consisting of nitrogen are used to form a nitridation layer 42 on the oxide layer 40 as shown in Fig. 2D. Preferably, in the nitridation process, the process temperature is 800~1000℃ (the best is 900℃), the process time is 90~120 minutes (the best is 100 minutes), and the gas used is NH_3. This completes a capacitor dielectric structure comprising the SiN layer 38, the oxide layer 40 and the nitridation layer 42.

Compared with the prior art of forming the capacitor dielectric structure, the present invention provides the nitridation process to form the nitridation layer 42 on a NO structure, thus increasing the dielectric constant and ensuring the electrical property of the capacitor dielectric structure. It is improved by experiments in which the capacitor dielectric structure enhances capacitance of a deep trench capacitor, prolongs data retention time of a deep trench capacitor, improving electrical properties of a deep trench capacitor, and increases yield. In addition, the present invention is applied to any other memory device process to achieve a capacitor dielectric structure with a high dielectric constant.

It is to be understood that the present invention is not limited to the embodiments described above, but encompasses any and all embodiments within the scope of the following

claims.